TUBF0304 Product Brief

1. Description

The TBUF0304 is an excellent clock buffer chip. It supports 1.5GHz frequency and 4 outputs with ultra-low delay and jitter. It is mainly used in applications such as low jitter, high-frequency clock / data distribution and level conversion.

The buffer can support input from 3 modes clock sources, such as single-ended clock or differential clock or crystal source.

The TBUF0304 can be allocated to two output groups A and B and one LVCMOS output.

Each channel output of A and B banks can be independently programmed to LVPECL, LVDS, HCSL or HIZ mode. The LVCMOS clock output is synchronized with the selected clock and can be enabled or disabled.

The TBUF0304 supports flexible voltage range. Both core voltage and IO voltage support 2.5V or 3.3V power supply.

2. Applications

- IT infrastructure (servers, storages)
- 5g communication
- Network system, including switches and routers
- Automotive electronics

3. Key Features

- Two inputs support including Single-Ended, Differential and Crystal
- 4 outputs support three modes including LVDS, LVPECL and HCSL
- Up to 1.5GHz Output Frequency for Differential Outputs
- Up to 200MHz Reference Output for LVCMOS
- Ultra-low Measured Jitter
- Low Delay from inputs to outputs channel
- Low Skew between outputs within different banks
- Flexible independent supply voltage of 3.3V/2.5V
- Lead-Free & Fully RoHS Compliant
- Industrial Temperature Support (-40℃ ~ 85℃)
- Environment-friendly without Halogen and Antimony
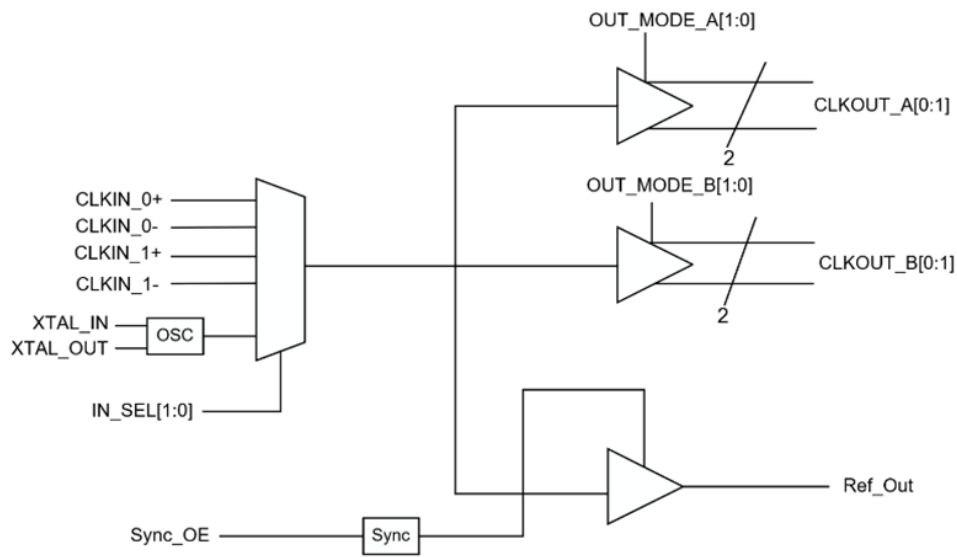- 32-pin, 5mm x 5mm QFN package

4. Functional Diagram
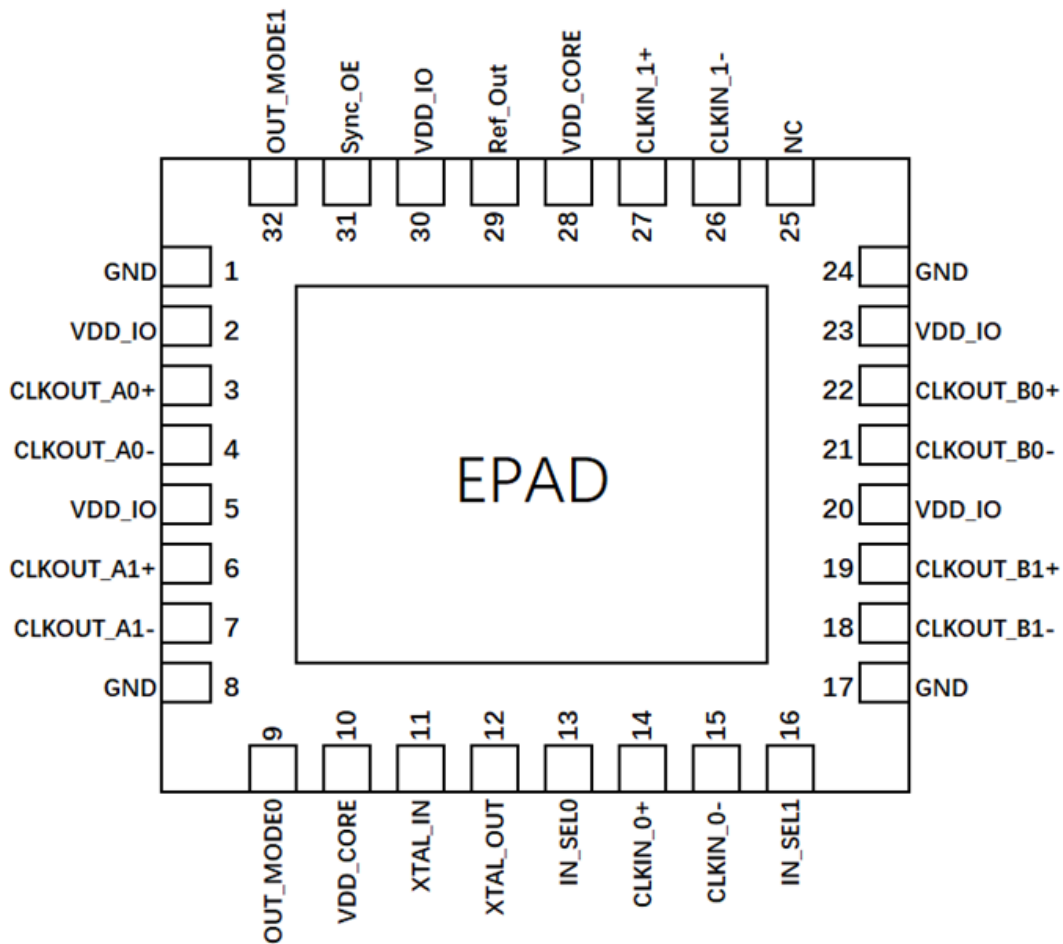

Figure 1 Functional Diagram

5. Pin Maps

Figure 2 Pin Assignment Diagram-QFN32

6. Pin Descriptions

Table 1 Pin Descriptions

Pin #	Pin Name	Type	Description
3, 4	CLKOUT_A0+ CLKOUT_A0-	Output	Differential clock output P/N of BANK A Channel 0. Can be configured by OUT_MODE_A pins.
6, 7	CLKOUT_A1+ CLKOUT_A1-	Output	Differential clock output P/N of BANK A Channel 1. Can be configured by OUT_MODE_A pins
2, 5, 20, 23, 30	VDD_IO	Power	Power supply pins for Output buffers.
1,8,17, 24	GND	Power	Ground pins.
9	OUT_MODE0	Input	Pulldown. output buffer type selection pins. View Table 3 for details.
32	OUT_MODE1	Input	
10, 28	VDD_CORE	Power	Power supply pins for core.
11	XTAL_IN	Input	Input pin for crystal supporting single ended input
12	XTAL_OUT	Output	Output pin for crystal. Leave XTAL_out OPEN if XTAL_in is driven by a single- ended clock.
13	IN_SEL0	Input	Pulldown. Clock input selections pins. View Table 2 for details.
16	IN_SEL1		
14	CLKIN_0+	Input	Universal clock input 0, built_in deviation to $0.33V_{DD\_CORE}$
15	CLKIN_0-	Input	Pullup/Pulldown.Reverse reference input 0, built_in deviation to $0.42V_{DD\_CORE}$
19, 18	CLKOUT_B1+ CLKOUT_B1-	Output	Differential clock output P/N of BANK B Channel 1. Can be configured by OUT_MODE_B pins.
22, 21	CLKOUT_B0+ CLKOUT_B0-	Output	Differential clock output P/N of BANK B Channel 0. Can be configured by OUT_MODE_B pins.
26	CLKIN_1-	Input	Pullup/Pulldown. Reverse reference input 0, built_in deviation to $0.42V_{DD\_CORE}$
27	CLKIN_1+	Input	Pulldown. Reverse reference input 0, built_in deviation to $0.33V_{DD\_CORE}$
29	Ref_OUT	Output	Reference output, CMOS
31	Sync_OE	Input	Pulldown. Synchronous output supports Ref_Out. View Table 4 for details.
25	NC	/	Disconnected pin
EPAD	EPAD	Gnd	Ground pins.